REMARKS

The claims are claims 1 to 4 and 11 to 14.

Claims 1 to 4 and 11 to 14 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Frankel et al U.S. Patent 4,463,443, Helen et al U.S. Patent 4,616,338 and Nakamura et al U.S. Patent 5,832,308.

The Applicant respectfully submits that the rejection of claims 1 and 14 as made obvious by the combination of Frankel et al, Helen et al and Nakamura et al fails to comply with the requirements of 37 CFR §1.104(c)(2). The text of 37 CFR §1.104(c)(2) states:

> "(2) In rejecting claims for want of novelty or for obviousness, the examiner must cite the best references at his command. When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified."

The application of the teachings of Helen et al to the limitations of claims 1 and 11 of this application refers to more than one column of the text (column 1, line 15 to column 2, line 28). The application of the teachings of Nakamura et al to the limitations of claims 1 and 11 of this application refers to plural figures (Figures 11 to 13) and nearly three columns of text (column 20, line 35 to column 23, line 17). No where does the rejection refer to particular reference numbers illustrated in Helen et al or Nakamura et al nor to any particular disclosed structure or signal. It is difficult for the Applicant to respond to a rejection which

cites plural columns of the reference as anticipating claimed elements. The Applicant respectfully submits that citation of at least one column of Helen et al and of Nakamura et al to the claim elements clearly fails the requirement that "the particular part relied on must be designated as nearly as practicable." This rejection likewise fails the requirement that "The pertinence of each reference, if not apparent, must be clearly explained." Thus the rejection fails to fulfill the requirements of 37 CFR §1.104(c)(2).

In particular, the response filed December 18, 2003 to the FINAL REJECTION of October 24, 2003 and the APPEAL BRIEF filed April 26, 2004 argued only a single limitation in claims 1 and 11 not shown in the primary reference Frankel et al. The Examiner needed only to find disclosure of a very specific limitation pointed out by the Applicant in the new secondary references Helen et al and Nakamura et al to sustain a rejection. Rather than point out particular structures or signals in the secondary references, the Examiner has made a generalized argument supported by reference to more than one column of Helen et al and to three figures and nearly three columns of Nakamura et al. The Applicant respectfully submits this rejection fails to meet the requirements of 37 CFR §1.104(c)(2).

The Applicant respectfully requests a more detailed application of the teachings of Helen et al and Nakamura et al to the features of the claims. The Applicant would greatly appreciate citation of individual reference numbers illustrated in the references for each claimed element. In addition, it would greatly help the Applicant to limit citations to the text of the references to no more than 10 to 15 lines. The Applicant believes that it is the duty of the Examiner under 37 CFR §1.104(c)(2) to provide such detail. The Applicant submits if the Examiner is unable to this

more detailed application of the teachings of the secondary references, this is evidence of unobviousness of the claims.

Claims 1 and 4 recite subject matter not made obvious by the combination of Frankel et al, Helen et al and Nakamura et al. Claim 1 recites a copy/access controller "operable to prompt said second component to access said second buffer when said data is copied from said first buffer." Claim 11 similarly recites "prompting said second component to access said data in said second buffer when said copying step is completed." These limitations are not made obvious by the combination of Frankel et al, Helen et al and Nakamura et al.

Helen et al states at column 2, lines 5 to 13 (within the portion cited in the FINAL REJECTION):

> "supplemental means for generating an internal reading request and directing it to said random access memory when said third storing means are in a condition indicating that the first output buffer register is empty and as long as said reading request has not been acknowledged, and for resetting said third storing means into a condition indicating that said first output register is loaded as soon as the reading request has been acknowledged"

This portion of Helen et al states that the reading request from the random access memory is generated "when said third storing means are in a condition indicating that the first output buffer register is empty and as long as said reading request has not been acknowledged." The Applicant respectfully submits that this condition for prompting reading out of the random access memory is neither the condition "when said data is copied from said first buffer" recited in claim 1 nor the condition "when said copying step is completed" recited in claim 11.

Nakamura et al discloses two uses of the FIFO full signal. Nakamura et al discloses the first use at column 20, lines 49 to 55 (within the portion cited in the FINAL REJECTION):

"Status 3: FIFO status verification. If the FIFO is not full, the DMA transfer control circuit proceeds to status 4. If it is full, the DMA transfer control circuit remains at status 3. In other words, data is output in this case from the buffer memory (DMA transfer control circuit) to the FIFO, as shown in FIG. 10, but if the FIFO is full, data cannot be input to the FIFO."

This disclosure teaches not transferring data into the FIFO when the FIFO is full. This clearly is a different disclosure than the above quoted limitation regarding prompting the second component to access the second buffer as recited in claims 1 and 11. Nakamura et al includes similar teachings at column 22, lines 51 to 53 and at column 26, lines 20 to 23. Nakamura discloses the second use at column 22, lines 1 to 6 (within the portion cited in the FINAL REJECTION):

"Status 7: If it is determined in status 6 that the FIFO is full, data is transferred from the FIFO to the buffer memory. In other words, after outputting the end imminent signal in status 5, the DMA transfer control circuit waits until the FIFO becomes full (status 6), then transfers data from the FIFO to the buffer memory once it has become full."

This disclosure teaches transferring data from the FIFO into the buffer memory when the FIFO is full. This is neither prompting a second component to access the second buffer "when said data is copied from said first buffer" recited in claim 1 nor prompting a second component to access the second buffer "when said copying step is completed" recited in claim 11. In order to teach these limitations, Nakamura et al would have to teach prompting reading of the buffer memory under these conditions. Nakamura et al fails to teach this subject matter. Accordingly, claims 1 and 11 are allowable over the combination of Frankel et al, Helen et al and Nakamura et al.

Claims 2 to 4 and 12 to 14 are allowable by dependence upon respective allowable base claims 1 and 11.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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